WHAT IS CLAIMED IS

1. A bootstrap circuit comprising a thin film transistor

wherein:

a channel forming region of the thin film transistor comprising a polycrystalline semiconductor, and

the thin film transistor is a depletion mode transistor.

2. The bootstrap circuit according to claim 1,

wherein the thin film transistor is directly connected to an output terminal.

3. The bootstrap circuit according to claim 1,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

4. A bootstrap circuit comprising a thin film transistor

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon, and

the thin film transistor is a depletion mode transistor.

5. The bootstrap circuit according to claim 4,

wherein the thin film transistor is directly connected to an output terminal.

6. The bootstrap circuit according to claim 4,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

7. A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a source follower

circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor, and

the thin film transistor is a depletion mode transistor.

8. The driver circuit according to claim 7,

wherein the thin film transistor is directly connected to an output terminal.

9. The driver circuit according to claim 7,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

10. A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a source follower circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon, and

the thin film transistor is a depletion mode transistor.

11. The driver circuit according to claim 10,

wherein the thin film transistor is directly connected to an output terminal.

12. The driver circuit according to claim 10,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

13. A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a bootstrap circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor, and

the thin film transistor is a depletion mode transistor.

14. The driver circuit according to claim 13,

wherein the thin film transistor is directly connected to an output terminal.

15. The driver circuit according to claim 13,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

16. A driver circuit comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a bootstrap circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon, and

the thin film transistor is a depletion mode transistor.

17. The driver circuit according to claim 16,

wherein the thin film transistor is directly connected to an output terminal.

18. The driver circuit according to claim 16,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

19. A display device comprising:

an insulating surface;

a signal line over the insulating surface;

a scanning line over the insulating surface;

a pixel electrically connecting to the signal line and the scanning line; and

a driver circuit electrically connecting to the scanning line, comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a bootstrap circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor, and

the thin film transistor is a depletion mode transistor.

20. The display device according to claim 19,

wherein the thin film transistor is directly connected to an output terminal.

21. The display device according to claim 19,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.

22. A display device comprising:

an insulating surface;

a signal line over the insulating surface;

a scanning line over the insulating surface;

a pixel electrically connecting to the signal line and the scanning line; and

a driver circuit electrically connecting to the scanning line, comprising:

a shift register;

a buffer circuit electrically connected to the sift register, comprising a bootstrap circuit comprising a thin film transistor; and

an analog memory electrically connected to the buffer circuit,

wherein:

a channel forming region of the thin film transistor comprises a polycrystalline semiconductor which is formed by crystallizing an amorphous silicon, and

the thin film transistor is a depletion mode transistor.

23. The display device according to claim 22,

wherein the thin film transistor is directly connected to an output terminal.

24. The display device according to claim 22,

wherein the polycrystalline semiconductor film is provided over either a quartz substrate or a glass substrate.